Abstracts

An analytic method to determine GaAs FET parasitic inductances and drain resistance under active bias conditions

C.F. Campbell and S.A. Brown. "An analytic method to determine GaAs FET parasitic inductances and drain resistance under active bias conditions." 2001 Transactions on Microwave Theory and Techniques 49.7 (Jul. 2001 [T-MTT]): 1241-1247.

An analytic technique to determine the parasitic inductances, source resistance, and drain resistance of the FET equivalent circuit is presented in this paper. The method exploits the frequency dependence of the extracted circuit parameters to determine the parasitic inductances and drain resistance from S-parameters measured over frequency for one active bias condition. Given a value for the parasitic gate resistance R/sub g/, all of the other equivalent-circuit parameters are uniquely extracted. The method is fast and robust, making it suitable for in-line statistical process tracking, as well as device modeling. A process tracking example for a 12-wafer 1864-device sample and FET modeling results up to 40 GHz are also presented.

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